Electrical Performance of Bumpless Build-Up Layer Packaging

Henning Braunisch, Steven N. Towle, Richard D. Emery,
Chuan Hu, and Gilroy J. Vandentop

Intel Corporation
Chandler, Arizona, USA

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Overview

BBUL overview

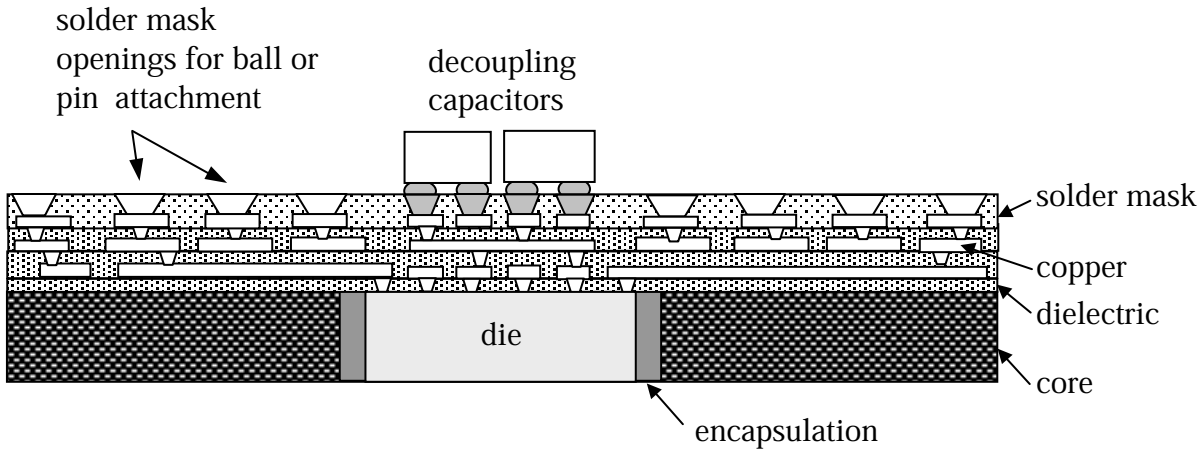
Lumped-element power delivery modeling

Transient 2.5-D simulations and results

Decoupling capacitors reduction study

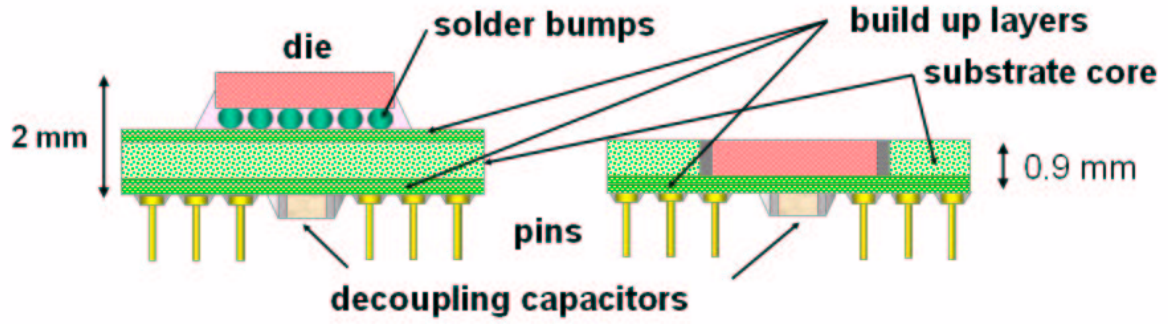
Conclusions

The bumpless build-up layer (BBUL) packaging concept



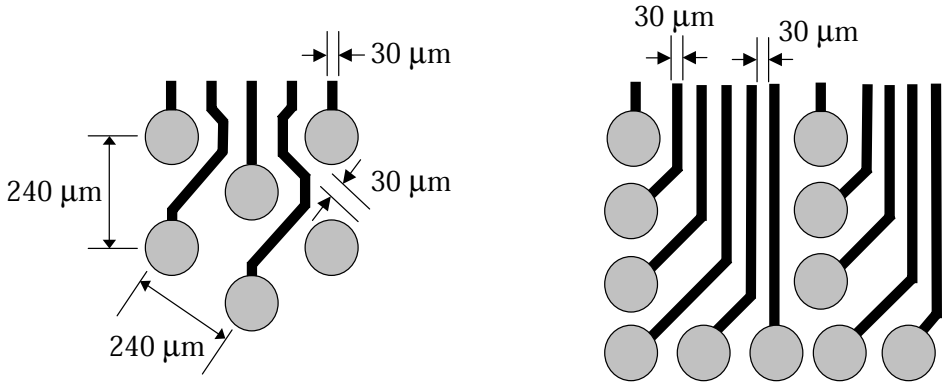
Schematic cross-section of a three-layer BBUL package.

Comparison of standard flip-chip and BBUL packaging



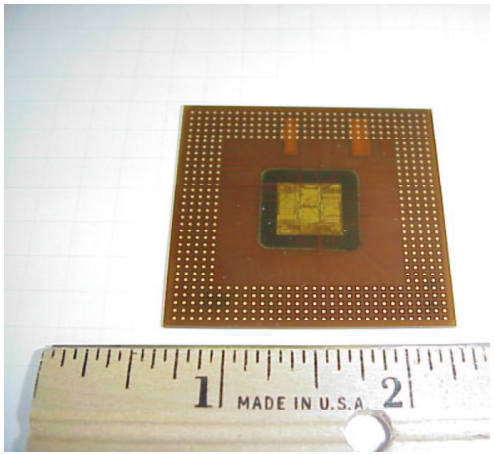
Standard	BBUL
Solder bumps, underfill	No bumps (more connections)
Two-sided substrate	Layers built up onto die
Thickness 2 mm	Thickness 0.9 mm
Capacitors more than 1 mm from die	Capacitors close to die (100 μm)

Escape routing

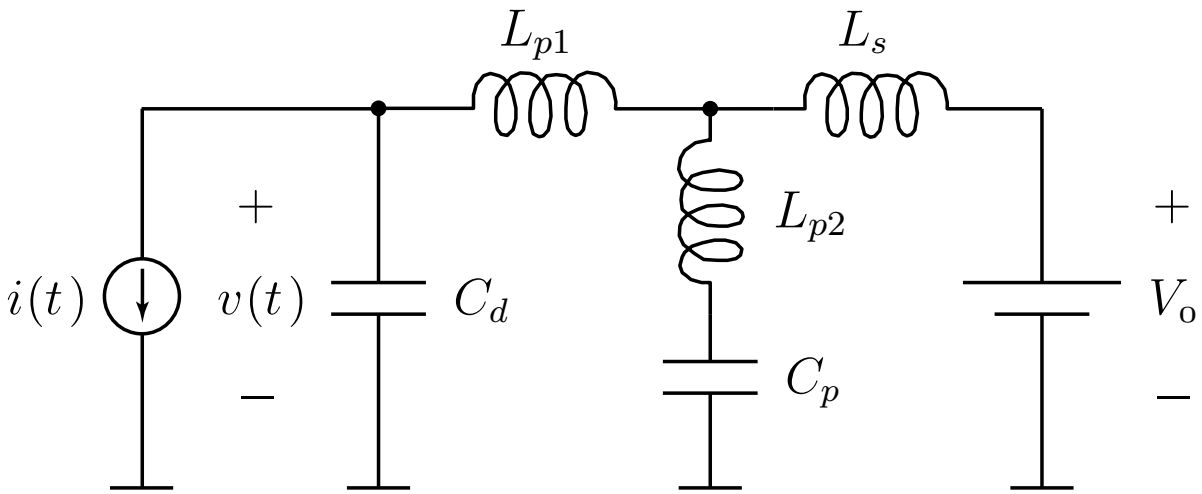


Standard package constrained to fixed pitch (left)
and BBUL package with equivalent design rules (right).

Views of BBUL test packages



Lumped-element power delivery modeling



Lumped-element model of a power delivery structure.

Die voltage droop theory

Transitions draw a large current from the package:

$$i(t) = I_0 + \Delta I \, u(t) \tag{1}$$

Initially L_s isolates the power supply from the rest of the circuit:

$$L_s \to \infty \ , \quad L_p = L_{p1} + L_{p2} \tag{2}$$

Solution to the initial-value problem:

$$v(t) = V_0 - \frac{\Delta I \, u(t)}{1 + C_d/C_p} \left[\frac{1}{\omega_0 \, C_d} \, \sin \omega_0 \, t + \frac{t}{C_p} \right] \tag{3}$$

with

$$\omega_0 = \sqrt{\frac{1/C_d + 1/C_p}{L_p}} \tag{4}$$

Limiting cases for voltage drooping

Initially, all charge is drawn from on-die capacitance C_d:

$$v(t) \sim V_0 - \Delta I \, \frac{t}{C_d} \quad \text{as} \quad t \to 0^+ \tag{5}$$

At late times:

$$v(t) \sim V_0 - \Delta I \, \frac{t}{C_d + C_p} \quad \text{when} \quad t \gg \frac{C_p}{\omega_0 \, C_d} \tag{6}$$

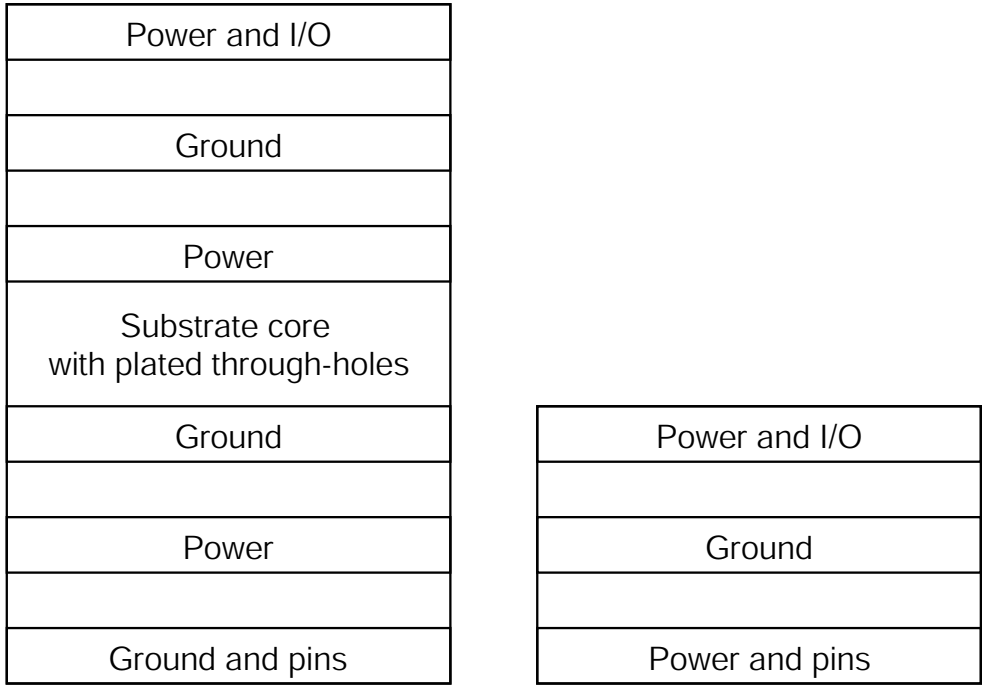
For typical microchips $C_p \gg C_d$ and as $C_p \to \infty$ [S&G, 1995]:

$$v(t) = V_0 - \Delta I \, u(t) \sqrt{\frac{L_p}{C_d}} \, \sin \omega_0 t \tag{7}$$

with

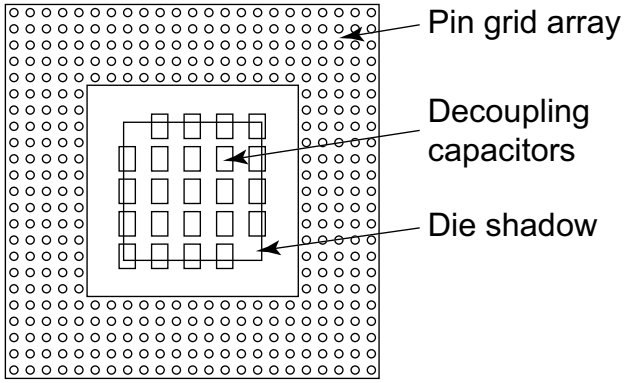
$$\omega_0 = \frac{1}{\sqrt{L_p \, C_d}} \tag{8}$$

Transient 2.5-D power delivery simulations



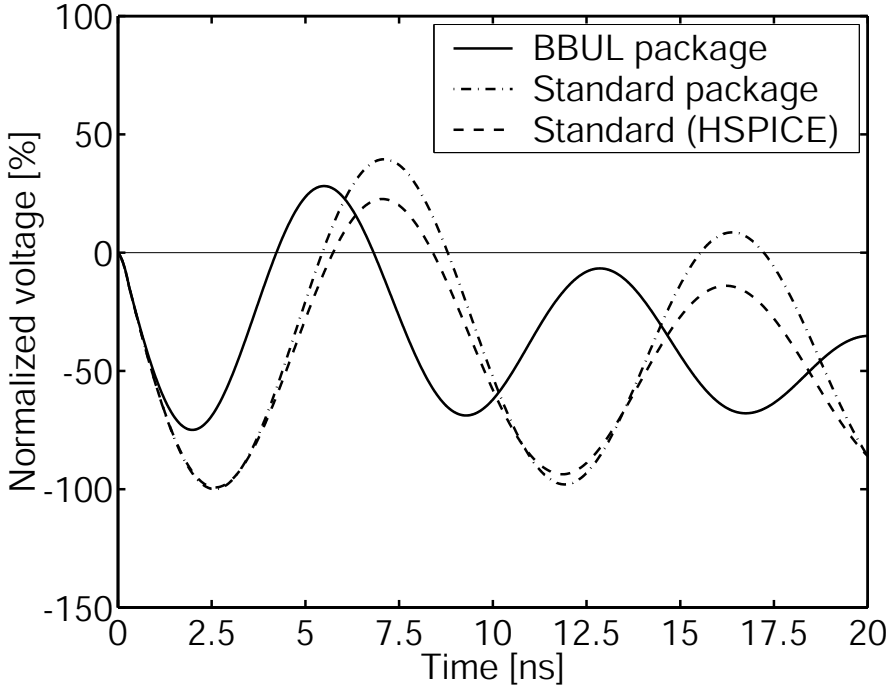
Stack-up of a standard six-layer package with a substrate core (left) and stack-up of a three-layer BBUL package (right).

Landside decoupling capacitors



Discrete decoupling capacitors populating the bottom of the two microprocessor packages with pin/ball grid array.

Transient simulation results



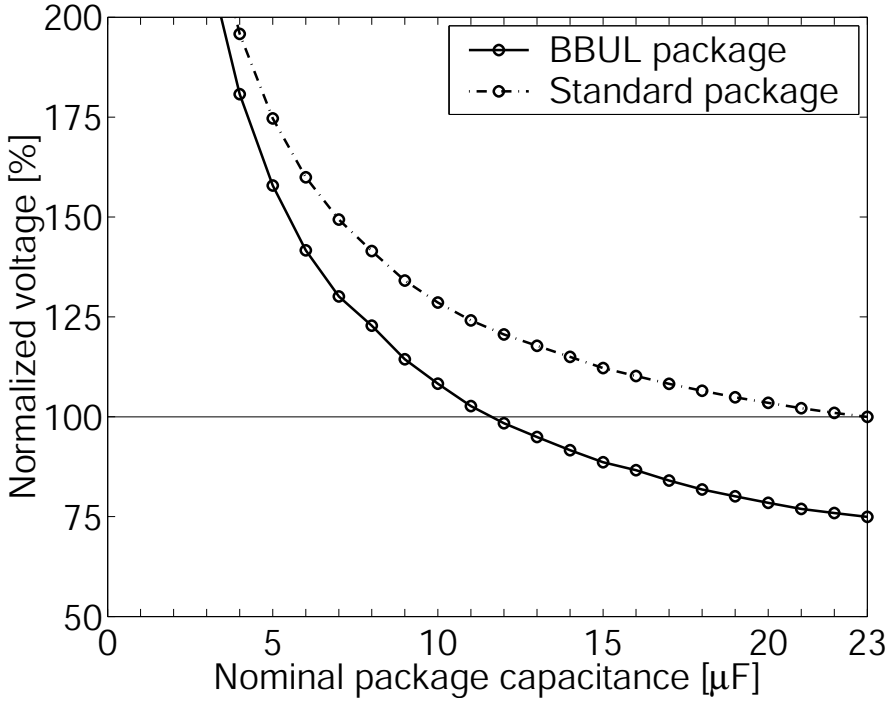
The mean die voltage of the two packages, together with HSPICE validation data.

Transient simulation results

- First voltage droop $\Delta I\sqrt{L_p/C_d}$ reduced by 25% .
- Effective loop inductance L_p reduced from $3.3\,$pH to $1.3\,$pH or by 61% .
- Effective package inductance L_{p1} reduced from $2\,$pH to $0.03\,$pH or by 98.5% .

  $\rightarrow$ The loop inductance in the case of BBUL is dominated by the equivalent series inductance (ESL) of the decoupling capacitors.
  $\rightarrow$ Optimize BBUL decoupling solution for higher performance or lower cost.

Decoupling capacitors reduction study



First voltage droop as simulated for the two packages with varying total decoupling capacitance.

Conclusions

- BBUL drastically reduces the package inductance for power delivery. Enables higher performance or lower cost.
- Thin packages call for a high-to-mid-frequency level in the power decoupling hierarchy, in between the on-die high-frequency decoupling and the on-package mid-frequency decoupling stages.
- BBUL provides minimized discontinuities for high-speed signaling (no PTHs, no die/substrate bumps, reduced layer count).